FingerChip®
AT77C108A

PRELIMINARY SPECIFICATIONS

Thermal Fingerprint sensor
Acquisition Navigation and Wake up functions
SPI interface

Features

Thermal Sensitive layer over a 0.35 µm CMOS array
Image zone: 0.3 x 9.6 mm
Image array: 6 x 192 = 1152 pixels
Image resolution: 508 dpi (50 µm x 50µm pixel pitch)
Serial Peripheral Interface (SPI) 16Mbps
Operating voltage range: 2.3V to 3.6V
Operating Temperature Range: -40ºC to 85ºC
Finger Sweeping speed from 2 to 35 cm/Second
Low Power: <5 mA (Image acquisition), <2 mA (navigation & click), <30 µA (Wake up), <10 µA (Idle mode)
Small Form Factor Packaging
High Protection from Electrostatic Discharge: +/-16 kV
Resistance to abrasion: >5 millions finger sweeps
Compliant with the European Directive for Restriction of Hazardous Substances (RoHS Directive)

Description

This document describes the specification of the AT77C108 FingerChip® sensor based on Atmel's proprietary thermal technology. This fingerprint sensor is part of the FingerChip family of linear sensor that captures fingerprint images by sweeping the finger over its sensing area.

Providing high quality images, ease of integration and touchpad navigation, the AT77C108 integrates smoothly into low power and highly demanding environments such as PC applications and Wireless systems.

Ultimately, this sensor associated with a dedicated FingerChip Security Processor provides state of the embedded biometrics operation in a highly secured environment protecting user's privacy.

Applications

- Notebook, PC-add on (Access Control, e-business)
- Scrolling, Menu and Item Selection for PDAs, Cellular or Smartphone Applications
- Cellular and Smartphone-based Security (Device Protection, Network and ISP Access, E-commerce)
- Personal Digital Agenda (PDA) Access
- User Authentication for Private and Confidential Data Access
- PIN Code Replacement
- Automated Teller Machines, POS
- Electronic Keys (Cars, Home, Government...)
- Portable Fingerprint Imaging for Law Enforcement
- TV Access

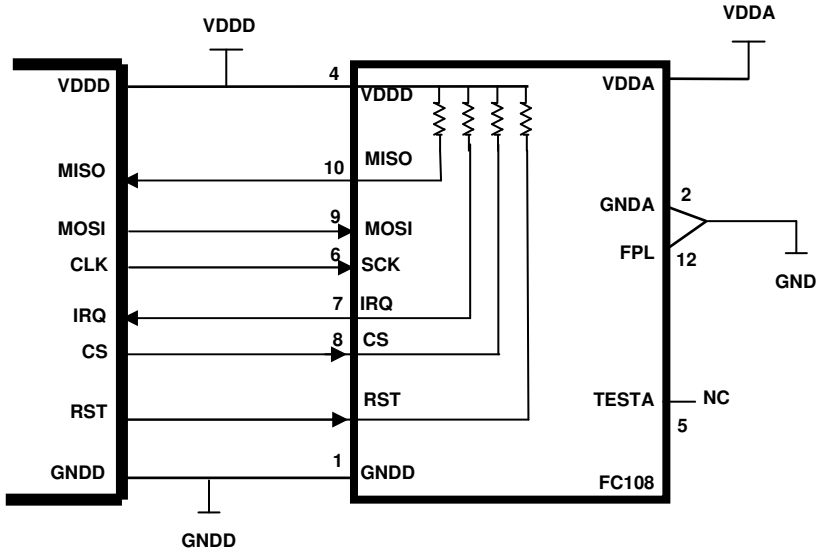
Molded Package

Pin Description for molded Package: AT77C108A-XXXXI

Pin Number	Name	Type	Description
1	GNDD	P	Digital Ground
2	GNDA	P	Analog Ground
3	VDDA	P	Analog Power Supply
4	VDDD	P	Digital Power Supply
5	TESTA	A_I/O	Analog test : only used in test mode
6	SCK	I	Clock (Up to 16 MHz)
7	IRQ	O	Wake-up interrupt pin (active LOW)
8	CS	I	SPI Chip select (active LOW)
9	MOSI	I	SPI Master Out Slave In pin
10	MISO	O	SPI Master In Slave Out pin
11	RST	I	SPI Reset (active LOW)
12	FPL	P	Must be connected to GNDA

Note: The die attach is connected to GNDA and must be grounded. The FPL pin must also be grounded.
TESTA pin is reserved for factory test and debug.

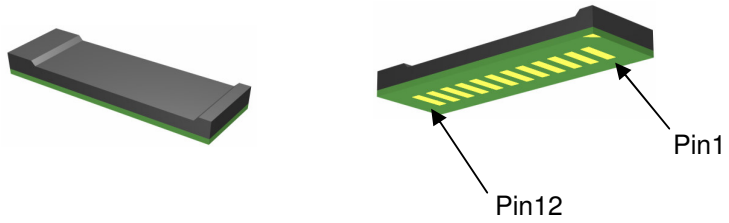
Typical Application



Companion chip (Master) **FC108 (Slave)**

Note: The noise must be lower than 30 mV peak-to-peak on VDDA and VDDD.

Pin Description



Specifications

Absolute Maximum ratings

Parameter	Symbol	Comments	Value	Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Power supply voltage	V_{DDD}, V_{DDA}		-0.5 to 4.6V	
Front Plane	FPL		G_{NDA}	
Digital Input	SCK, RST,MOSI, CS		G_{NDD} to V_{DDD}+0.5V	
Storage temperature	Tstg		-40 to +85°C	
Lead temperature	Tleads	Do not solder	**Forbidden**	

Recommended conditions of use

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	V_{DD}	V_{DD}=V_{DDD}=V_{DDA}	2.3	2.5 3.3	3.6	V
Front plane	FPL	Must be connected to G_{NDA} and grounded	G_{NDA}			V
Digital input voltage			CMOS levels			V
Digital output voltage			CMOS levels			V
Digital load	C_L			20	50	pF
Operating temperature range	T_{amb}	Industrial	-40 to +85			°C

Resistance

Parameter	Min value	Standard method
ESD		
On pins. HBM (Human Body Model) CMOS I/O	2 kV	MIL-STD-883- method 3015.7
On die surface (Zap gun) Air discharge Contact discharge	 +/- 16 kV +/- 8 kV	NF EN 6100-4-2
MECHANICAL ABRASION		
# Cycles without lubricant Multiply by a factor of 20 for correlation with a real finger	250 000	MIL E 12397B
CHEMICAL RESISTANCE		
Cleaning agent, acid, grease, alcohol	4 hours	Internal method

Explanation of Test Levels

Level	Description
I	100% production tested at +25°C
II	100% production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample)
III	Sample tested only
IV	Parameter is guaranteed by design and/or characterization testing
V	Parameter is a typical value only
VI	100% production tested at temperature extremes
D	100% probe tested on wafer at T_{amb} = +25°C

Table 6 Specifications

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Resolution		IV		50		Micron
Size		IV		6 × 192		Pixel
Yield: number of bad pixels		I			5	Bad pixels
Equivalent resistance on TPP pin		I	25	30	45	Ohm

Power Consumption and DC Characteristics

The following characteristics are applicable over the operating temperature range. Testing conditions are: power supply = 3.3V; Tamb = 25°C; SCK = 16 MHz; duty cycle = 50%; CLOAD 120 pF (tester load) on digital outputs unless otherwise specified.

Power Requirements

Name	Parameter	Conditions	Test Level	Min	Typ	Max	Unit-
V_{DD}	Positive supply voltage	$V_{DD}=V_{DDD}=V_{DDA}$	I	2.3	2.5/3.3	3.6	V
I_{IDLE}	Idle mode		I			10	µA
I_{DD}	Acquisition mode		I			5	mA
I_{DD}	Navigation mode		IV			2	mA
I_{DDWU}	Wake up mode		I			30	µA
I_{HEAT}	With contrast enhancement		I			60	mA

Digital Inputs

Logic Compatibility		CMOS					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
I_{IL}	Low level input current without pull-up device	V_I = 0V	I			1	µA
I_{IH}	High level input current without pull-down device	$V_I = V_{DD}$	I			1	µA
I_{ioz}	Tri-state output leakage without pull up/down device	V_I = 0V or V_{DD}	IV			1	uA
V_{il}	Low level input voltage		I			0.3 Vdd	V
V_{ih}	High level input voltage		I	0.7 Vdd			V
V_{hyst}	Schmitt trigger hysteresis	V_{DD} = 3.3V Temp = 25°C	IV	0.40		0.75	V

Digital Outputs

Logic Compatibility		CMOS					
Name	**Parameter**	**Conditions**	**Test Level**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Low level output voltage	I_{OL} = 3 mA V_{DD} = 3.3V ±10% I_{OL} = 1.75 mA V_{DD} = 2.5V ±5%	I			0.15 V_{DD}	V
V_{OH}	High level output voltage	I_{OH} = -3 mA V_{DD} = 3.3V ±10% I_{OH} = -1.75 mA V_{DD} = 2.5V ±5%	I	0.85 V_{DD}			V

Switching performances

The following characteristics are applicable over the operating temperature range. Testing conditions are: power supply = 3.3V; Tamb = 25°C; SCK = 16 MHz; duty cycle = 50%; CLOAD 120 pF (tester load) on digital outputs unless otherwise specified.

Timings

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Clock frequency	F_{SCK}	IV			16	MHz
Duty cycle (clock SCK)	DC	IV	20	50	80	%
Reset setup time	T_{RSTSU}	I	½ T_{SCK}(1)			ns
Select setup time	T_{SSU}	I	½ T_{SCK} (1)			ns
Select Hold time	T_{SHD}	I	½ T_{SCK} (1)			ns

(1) $T_{SCK} = 1/F_{SCK}$ (clock period)

3.3V ±10% Power Supply

Parameter	Symbol	Test Level	Min	Typ	Max	Unit
Data in setup time	T_{SU}	IV		3		ns
Data in hold time	T_H	IV		1		ns
Data out valid	T_V	I			30	ns
Data out disable time from CS high	T_{DIS}	IV		4		ns
IRQ out valid	T_{IRQ}	IV		80 See (1)		us

Note: All power supplies = +3.3V
(1) The IRQ wire is put low typically 80us after the finger detection. This IRQ wire stays low until the chip return in Idle mode.

Timing Diagrams

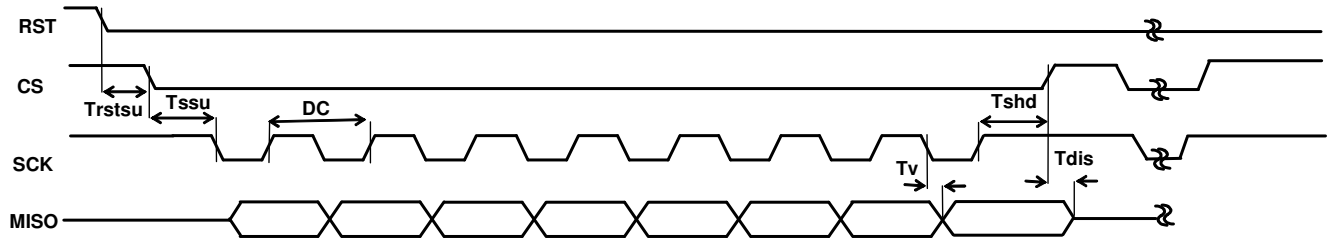


Figure: read timing

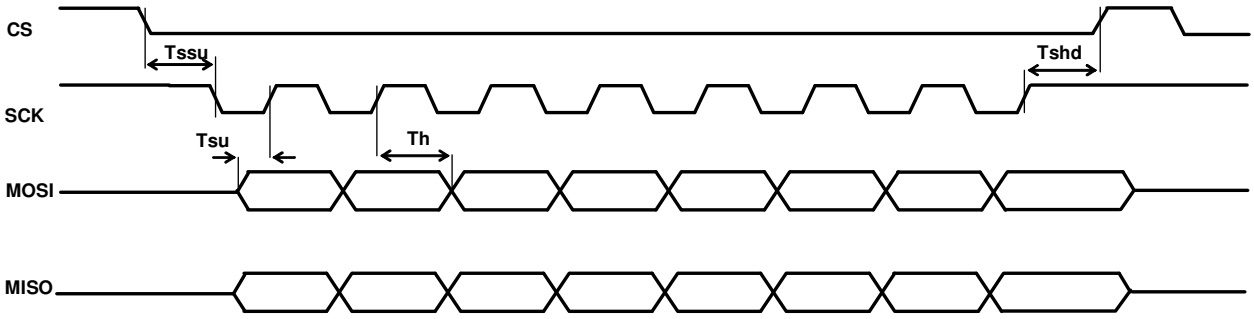


Figure: read/write timing

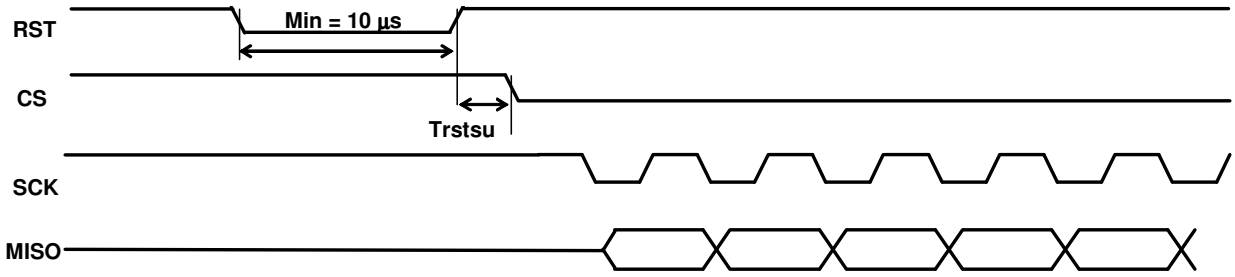
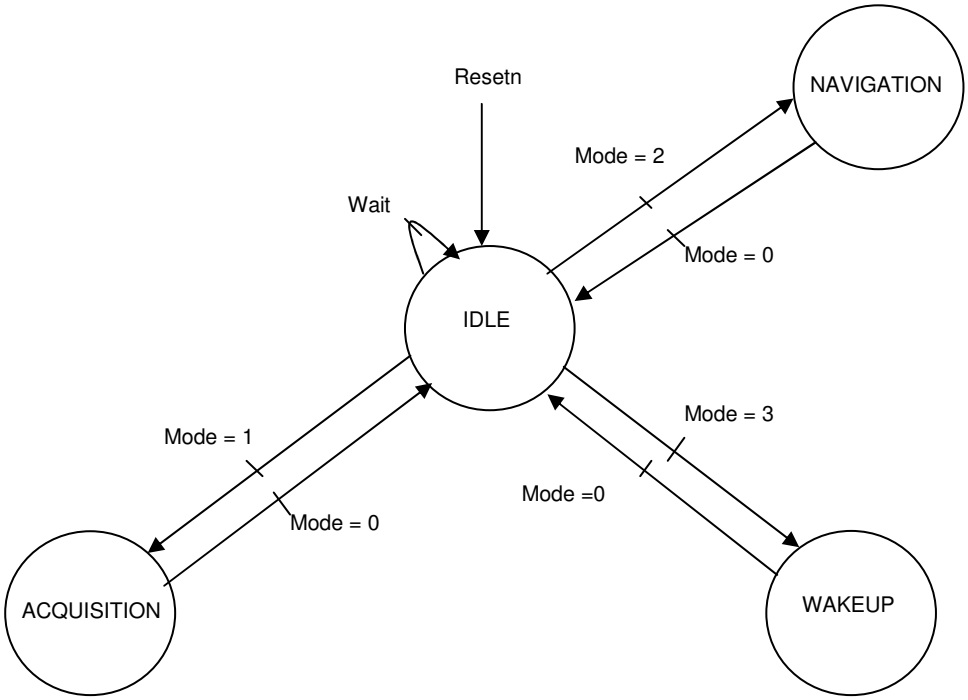


Figure: chip initialization

Functional Description

Architecture – State machine



AT77C108A is a fingerprint sensor based on FingerChip® technology. It is controlled by a SPI serial interface and output data are also transferred through a SPI interface.
Four modes have been implemented:

Start Sequence/Idle mode (mode 0)
The first requested order from the Host is to activate the reset pin RST. This value keeps the low level for 10µs minimum. At this moment, understand: “during reset activation”, the FC108 is set in IDLE mode.
The FC108 is now waiting instructions from the companion chip.

Acquisition mode (mode 1)
This mode is used to generate fingerprint slices directly from the device. From this mode the user is able to call for a user friendly fingerprint data acquisition.
In this mode, the 192 x 6 pixels array is used.
As long as the finger is touching sensor, the full acquisition speed is required. The frame integration time should be between 0.5 and 1 ms corresponding respectively to a 2000 to 1000 slices /second.

Navigation & click mode (mode 2)
In this mode the AT77C108 reacts like a touchpad. It allows for sensing X, Y motions and click actions that are usable by the Operating System through the companion chip or a standard driver layer.
In this mode, 128 x 6 pixel array is used (columns 32 to 159).
Additionally, the navigation and click data go through the application driver layer that can further process or rearrange them at wish giving more freedom to the end user in the use of these data.

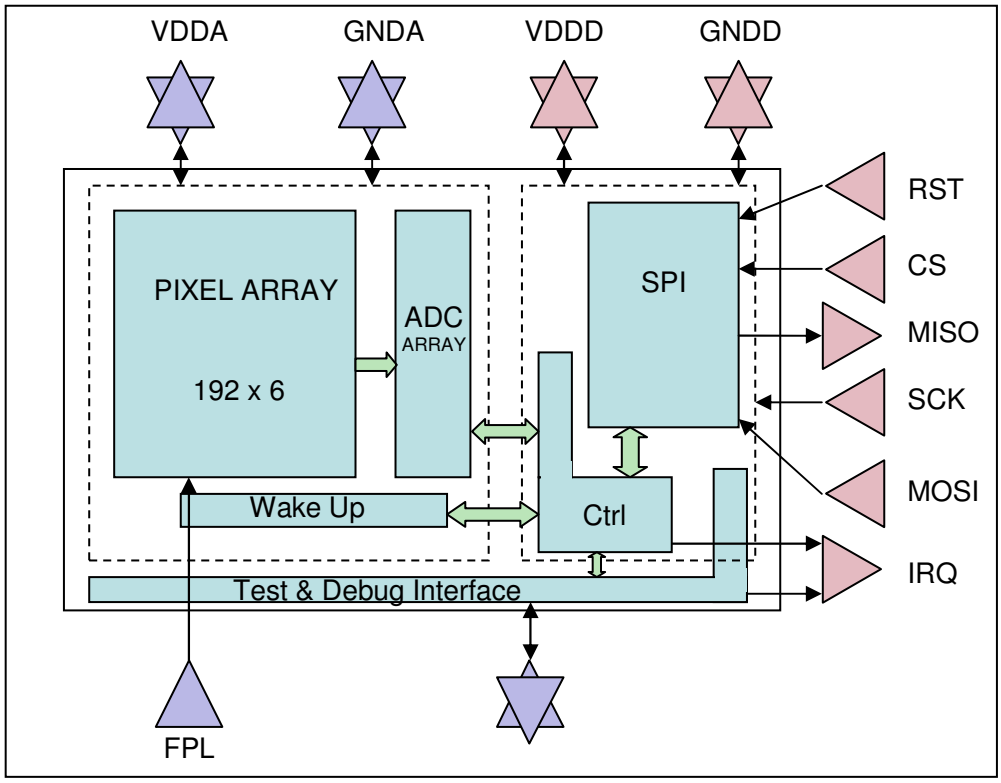
During this loop, the full acquisition speed is not required. The FC108 exits from this navigation mode only when its returns in IDLE mode.

Wake Up detection (mode 3)
Wake up mode is a mode where very low power consumption can be achieved at system level.
This mode allows the update of an interrupt upon detection of a finger swipe, or exit by holding the idle register.
Once the finger is detected, the interrupt pin is pushed down and the WU_Status set to 1.
This mode does not generate any image but it can be followed by an immediate slices acquisition.

Note: The term “host” or “master” or “companion chip” describes the main master processor (controller, DSP...) linked to the sensor.

Sensor and Bloc Diagram

Functional Block Diagram



The Circuit is divided into the following main sections:

- Array or frame of 6 x 192 pixels +1 dummy column,
- Analog to digital conversion,
- On chip oscillator, control and status registers,
- Wake up
- Control and interface mode (SPI)

Function registers

Communication Interface Registers:
Next list gathers register used for communication interface management.

@	Rst	Access	Mnemonic	Description
Miscellaneous Control/Status Register				
0x00	0x00	RW	CTRL	Control Register
0x01	0x00	RW	ANA_TEST(1)	Analog Test configuration register
0x02	0x00	RW	DIG_TEST(1)	Digital Test configuration register
0x03	0x00	RW	Threshold_WU	Wake up Threshold register
0x04	0x00	RW	Time_ WU	Wake up time register
0x05	0x00	RW	status _WU	Wake up status register

(1) Reserved for factory test and debug

Registers Description:

Control Register (CTRL @ 00h)

Bit	7	6	5	4	3	2	1	0
Mnemonic		HEAT		OSC	RSTPNEN	TEST_Mode	Mode	
Type		RW		RW	RW	RW	RW	
Reset		0x00		0x00	0x00	0x00	0x00	

Bit	Mnemonic	Description
7		
6:5	HEAT (1)	Heating 0x00 : OFF 0x01 : ON: 60mA consumption mode 0x02 : Reserved 0x03 : Reserved
4	OSC (2)	Oscillator Control: 0x00: Off 0x01: On
3	RSTPNEN	Permanent pixel reset enable (active low): when on, permanent pixel reset (RST_PERM) is forced to '1' during the first 80th pixels of the first slice: 0x00: On 0x01: Off
2	TEST MODE	Test mode Control: Do not used, reserved for factory test and debug 0x00: Off 0x01: On
1:0	Mode	Mode: 0x00: Idle 0x01: Acquisition 0x02: Navigation 0x03: Wake-Up

(1) A watchdog is implemented to control the heat time. When heating of the sensor is required, the sensor is heated during n seconds :

2.67 s (min) < n=4.00 s (typ) < 8.00 s (max)

Note: the oscillator has to be activated first when heating is required.
Note: heating is stopped when oscillator is stopped.
Note: there are 2 reasons to have bits 6 and 5 of the CTRL register cleared (when reading the control register):

- oscillator is off
- the watchdog has automatically cleared the bits

Threshold Wake Up Register (Threshold_WU @ 03h)

Bit	7	6	5	4	3	2	1	0
Mnemonic		WURVH		WURVB		WU_EVENT_TH		
Type		RW		RW		RW		
Reset		0x00		0x00		0x00		

Bit	Mnemonic	Description
7		
6:5	WURVH	Wake Up analog High threshold** 0x00 : 13 lsb equivalent 0x01 : 12 lsb equivalent 0x02 : 10 lsb equivalent 0x03 : 8 lsb equivalent
4:3	WURVB	Wake Up analog Low threshold** 0x00 : 2 lsb equivalent 0x01 : 3 lsb equivalent 0x02 : 4 lsb equivalent 0x03 : 6 lsb equivalent
2:0	WU_EVENT_TH	Numbers of Wake Up events** 0x00 : 1 event; 0x01 : 4 events; 0x02 : 8 events; 0x03 : 10 events; 0x04 : 12 events; 0x05 : 14 events; 0x06 : 16 events; 0x07 : 32 events;

** See “Wake up: functional description” below

Time Wake up Register (Time_WU @ 04h)

Bit	7	6	5	4	3	2	1	0
Mnemonic		-	-	-	-	WU_TI	WU_EVENTS_TI	
Type		-	-	-	-	RW	RW	
Reset		-	-	-	-	0x00	0x00	

Bit	Mnemonic	Description
7		
6:3		
2	WU_TI	Integration time for the Wake Up** 0x00 : 24 clock integration times (equivalent at 600 µs) 0x01 : 48 clock integration times (equivalent at 1.2 ms)
1:0	WU_EVENTS_TI	Time between two events** 0x00 : 3600 clock integration times (equivalent at 90 ms) 0x01 : 4992 clock integration times (equivalent at 125 ms) 0x02 : 6000 clock integration times (equivalent at 150 ms) 0x03 : 7200 clock integration times (equivalent at 180 ms)

** See “Wake up: functional description” below

Status Wake Up Register (Status_WU @ 05h)

Bit	7	6	5	4	3	2	1	0
Mnemonic		-	-	-	-	-	-	WU_Status
Type		-	-	-	-	-	-	R
Reset		-	-	-	-	-	-	0x00

Bit	Mnemonic	Description
7		
6:1	-	
0	WU_Status(1)	Status for Wake Up Interrupt 0x00 : Interrupt not activated (default value) 0x01 : Interrupt present.

Note1: wake-up status WU_STATUS is cleared when wake-up mode is deselected.

SPI Interface General Description

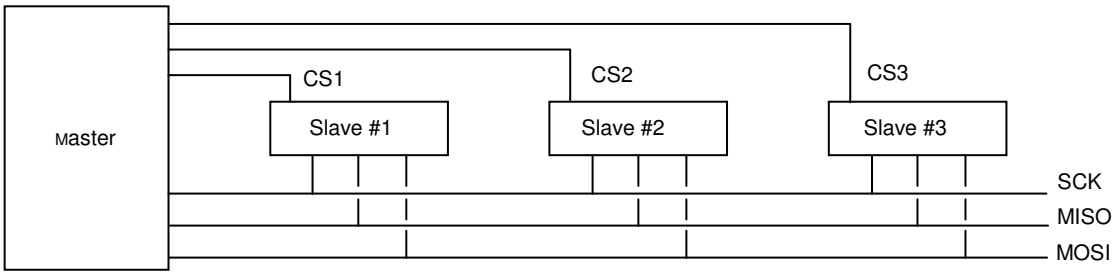
A synchronous Serial Port Interface (SPI) is implemented for the communications.
The SPI protocol is a multi-slaves/only-one-master full duplex synchronous serial communication.
This protocol uses 3 communication signals:

- SCK (Serial Clock) : the communication clock
- MOSI (Master Out Slave In) : the data line from master to slaves
- MISO (Master In Slave Out) : the data line from slaves to master

The slaves are selected by an input CS (Chip Select) which is active low. A master can communicate with several slaves.

Transfers
The word length of the transferred data is fixed to 8 bits. Most Significant Bit (MSB) is sent firstly. For each 8-bits transfer, there are 8 bits sent from the master to the slave and 8 bits transferred from the slave to the master. Transfers are still synchronized with the communication clock (SCK). Transfers can only be initialized by the master. Slave has to wait for a master's access to send data. When there is no transfer, no clock is generated.

One master with several slaves



SPI configuration - Example

When a master is connected with several slaves, the SCK, MISO and MOSI signals are interconnected. Each slave CS is separately driven. Only one slave can be selected: the others slaves have their MISO tri-stated and ignore MOSI data.
The CS signal must fall a half-period before the first clock edge (whatever the phase (see next paragraph)). It must rise a half-period after the last clock edge.

Clock phase and polarity

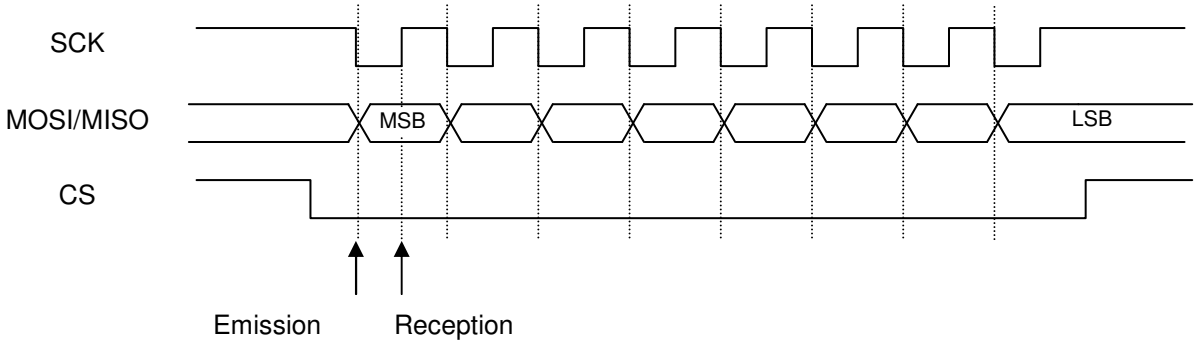
During phase 0 operation, output data changes on the falling clock edge, and input data is shifted in on rising edge. In phase 1 operation, output data changes on the rising edge of the clock and is shifted in on falling edge.

The polarity configures the clock idle level. Clock idle level is high (‘1’) during polarity 1 operation. Clock idle level is low (‘0’) during polarity 0 operation.

The FC108 supports only one phase and polarity configuration:

- Idle clock level is high (**polarity=1**).
- Output data change on the falling clock edge, and input data is shifted in on rising edges (**phase=0**).

SPI wave form (phase=0, polarity=1)



Note: during the initialization of the SCK wire (power-on or reset), CS must be inactive (‘1’).

SPI behavior with hazardous access

- SPI uses an internal finite state machine (FSM) which can only be initialized by the RST pin (asynchronous reset). When SPI access does not use 8 clock pulses, the internal FSM is desynchronized. The only way to synchronize it is to reset the FC108 with the RST pin.
- If a new command is sent just after a first one, the first one is ignored.

Control interface

This interface controls the internal registers of the sensor. The protocol enables the reading and the writing of these registers.
The master (the host) initiates transfers to the slave (the Sensor). The Sensor can only use its interrupt pin to communicate with the host.
The word length of the transferred data is fixed to 8 bits. Most Significant Bit (MSB) is sent firstly.

Communication protocol
Host accesses are structured in packet of words. The first word is the command. The other words are the data.
"b7" bit will be used to distinguish between the command and the data. When the word is a command, b7 bit is high ('1'). When the word is a data, b7 bit is low ('0').
The following protocol is used:

- Command: **the host indicates to the sensor if it wants to read or to write into a register and it indicates the address of the register.**

b7	b6	b5	b4	b3	b2	b1	b0
1	Read (1)/Write (0)	Address (b3)	Address (b2)	Address (b1)	Address (b0)	X	X

Command format

- Data :
  - **In the case of writing into a register, the host transmits the data.**

b7	b6	b5	b4	b3	b2	b1	b0
0	Data (b6)	Data (b5)	Data (b4)	Data (b3)	Data (b2)	Data (b1)	Data (b0)

Data format (writing into register)

  - **In the case of a reading of a register, the host must transmit one or several data, only to shift in the data from the sensor. The host must transmit dummy word with the data format (b7 bit is low ('0')).**

b7	b6	b5	b4	b3	b2	b1	b0
0	X	X	X	X	X	X	X

Data format (reading of register)

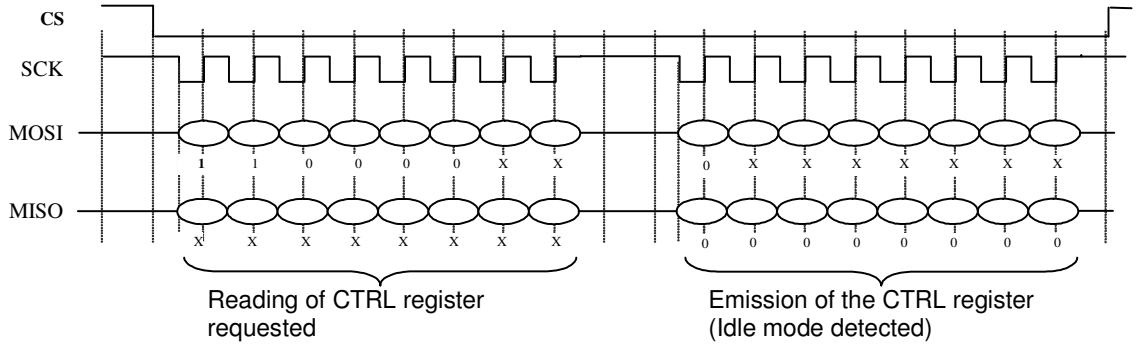
Note: the host cannot communicate with the sensor without receiving data from the sensor. The host will ignore uninteresting data from the sensor or with break between 2 transactions.

Example for the CTRL register

Register reading

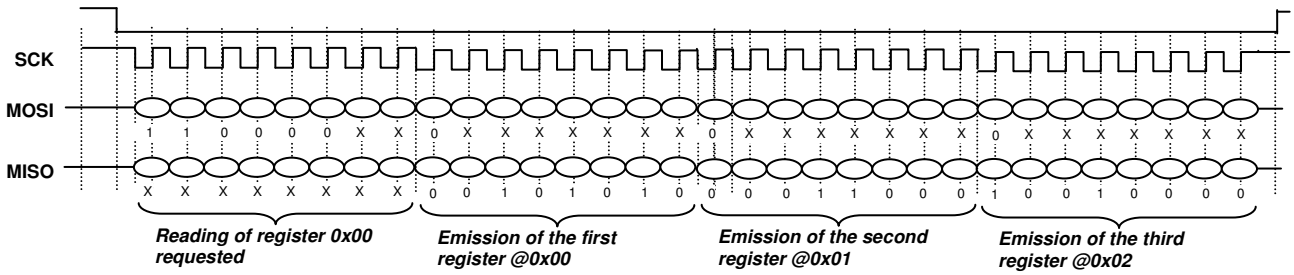
- Single read

Following chronogram represents a typical single reading sequence.



- Multiple read

Following chronogram represents a typical multiple reading sequence.



Writing into register

- Only available in single mode: To write into 2 registers, the user has to send 2 write commands.

Following chronogram represents a typical writing sequence into an internal register (CTRL register in this example).

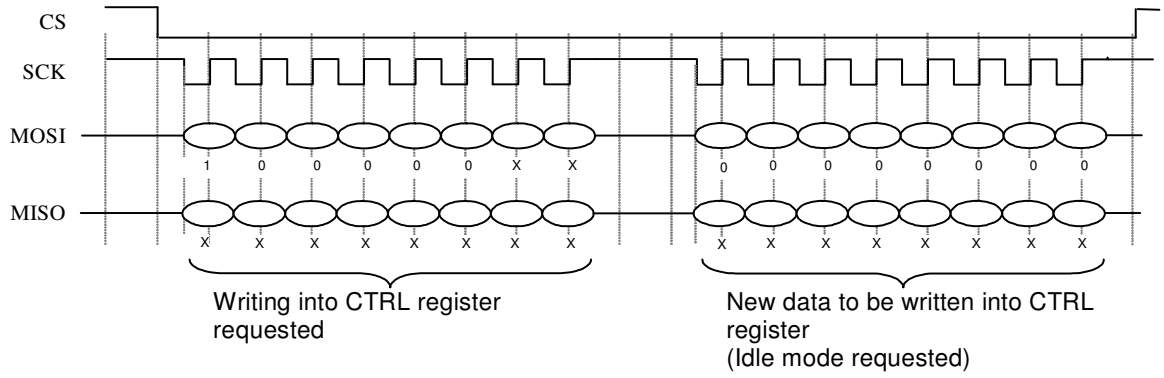
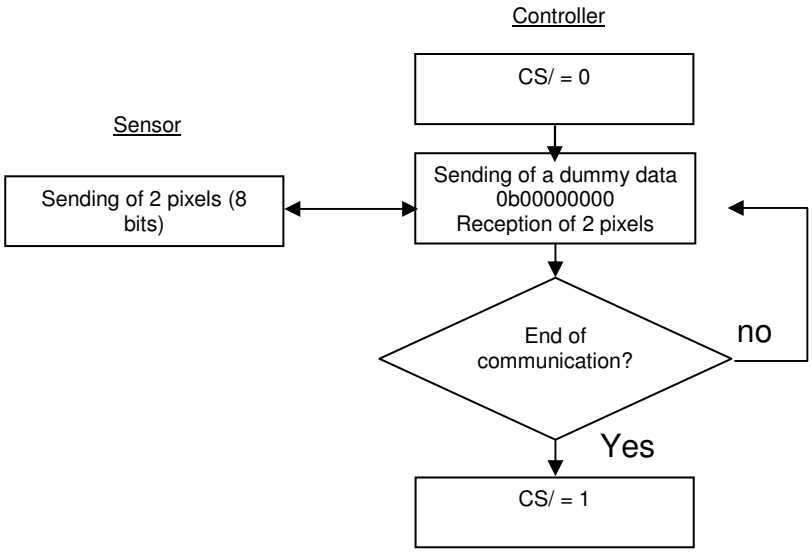


Image capture

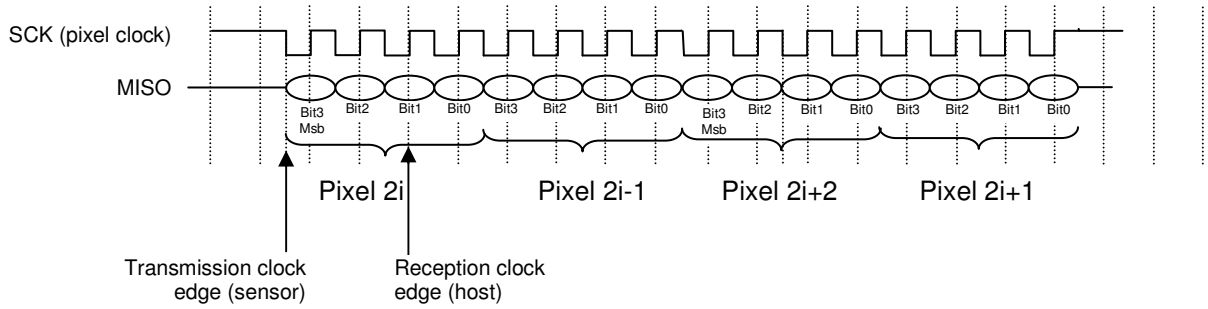
This interface (SPI) allows the acquisition by the host of the pixels of the sensor in acquisition mode. This serial interface only supports the serial clock (SCK) and one data line: MISO (Master In – Slave Out).

Communication protocol

When the sensor is in acquisition mode, the host can receive pixels.
The host has to transmit the communication clock (SCK) to receive pixels.



SPI communication



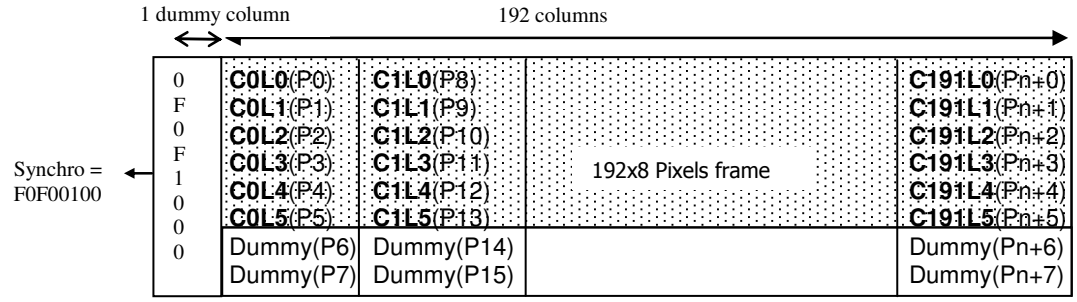
Communication speed
The pixels acquisition speed is linked with the communication clock speed. The faster the communication clock, the faster the authorized maximum finger speed. The sensor supports fast communications up to **16Mbps**.

Sensor
Each pixel is a sensor itself. The sensor detects a temperature difference between the beginning of the acquisition and the reading of the information: this is the integration time. The integration time begins with an internal reset of the pixel to a predefined initial state.
Note that the integration time reset has nothing to do with the reset of the digital section.
Then, electrical charges are generated at a rate depending on the temperature variation between the reset and the end of the integration time, and on the duration of the integration time, nominally 1 ms.

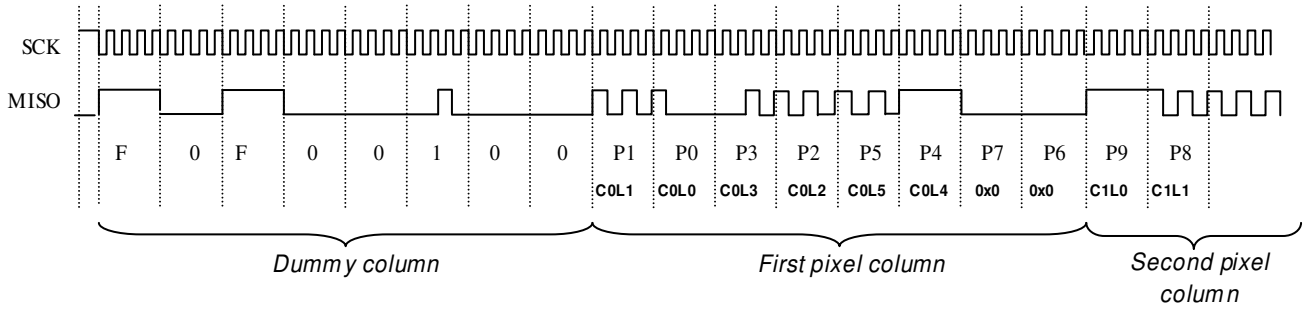
Analog to Digital Converter
An Analog-to-Digital Converter (ADC) is used to convert the analog signal coming from the pixel into digital data understandable by interface protocol.

Reading of frame
Each frame contains a 192 real columns and 1 dummy column used for synchronization. Each real column contains the values of 6 real and 2 dummy pixels.

Example of a Frame



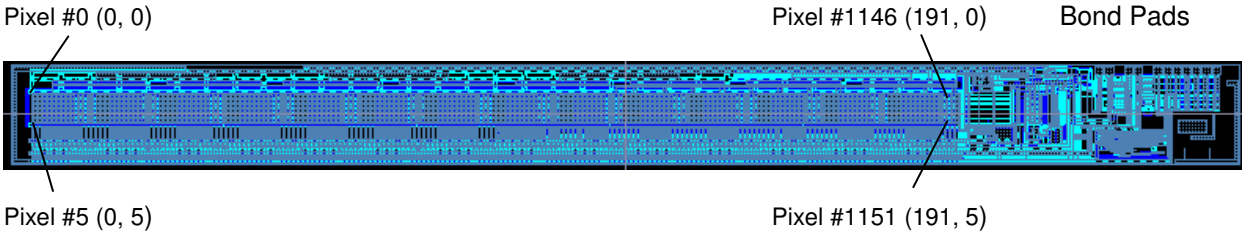
The first dummy column, at the beginning of the pixel array, is added to the sensor to act as a specific pattern easy to detect and used as start-of-frame tag. So, synchronization column is presented on the MISO output by the sequence F0F00100.



Note 1: **For the first array or frame reading, 40 dummy clock cycles must be sent before the first data arrives**. This is necessary for the initialization of the chip pipeline. So the first synchronization sequences will appear after 40 clock cycles. For the next array reading, data arrive at each clock cycle. It is advised to implement a synchronization routine in the protocol so as to look for the F0F00100 pattern.
Note 2: Most Significant Bit (MSB) is sent firstly

Pixel Order

The pixel array is always read in the following order: the 1st byte contains the value of the two pixels physically located on the upper left corner of the array, when looking at the die with bond pads to the right. The 2 following bytes contain the value of the 4 pixels physically on the same vertical row from up to down, following by 2 bytes set to 00(dummy bytes). Then, the next row on the right is output, and so on, until the last line on the right is output.



Description of fingerprints slices (or frame)

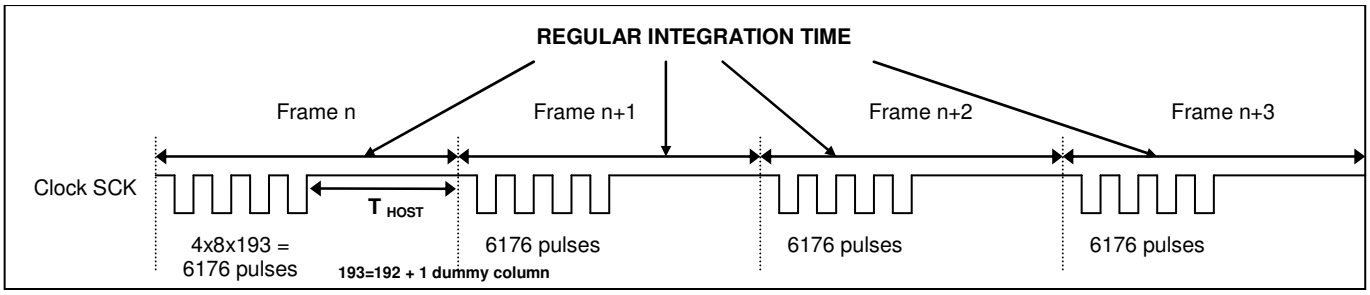
FingerChip® will deliver fingerprints slices (or frames) of (6 real and 2 dummy) x192 pixels. Pixels are sampled/read sequentially and synchronous with SCK. Raw slices are captured by acquisition system and overlapped with the corresponding X, Y finger displacement computed by ATMEL reconstruction software.
The table below describes finger speeds according to the different clock frequencies. In the table reconstruction is done after all slices acquisition, assuming 2 pixels recovery between slices.

Maximum finger speed vs Clock Frequency / 2 pixels recovery / no time delay between 2 slices

Fsck (MHz)	Data rate (Mbit/s)	Slices rate (Slices/s)	Maximum finger speed (cm/s)	Comments
1	1	162	3	Too slow
2	2	324	6	Too slow
4	4	648	12	Minimum
6	6	972	18	Normal speed
8	8	1295	24	Good speed
12	12	1944	36	Very good speed
16	16	2592	48	Very good speed

Integration Time
Basic data unit transfer is defined as a slice, which means that a slice is transferred from the FingerChip® to the host processor at each data transaction. Analog value for each pixel coming from sensor is digitized on 4 bits, which requires 32 clock pulses.

So, each frame of the FC108 will deliver slices of 8 x (192+1) x 4 bits = 6,176 bits, but useful data size containing fingerprint data is 6x192x4=4608 bits.

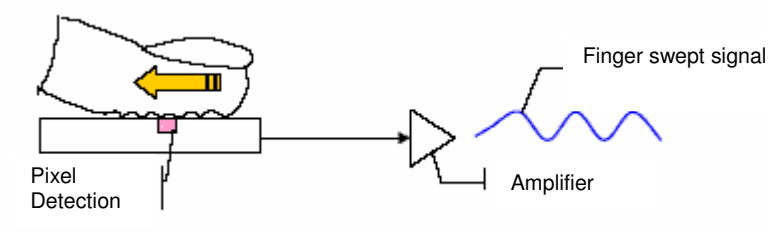


Note: T_{HOST} corresponds to some computation time achieved by the Host (slice reconstruction, finger detection…).

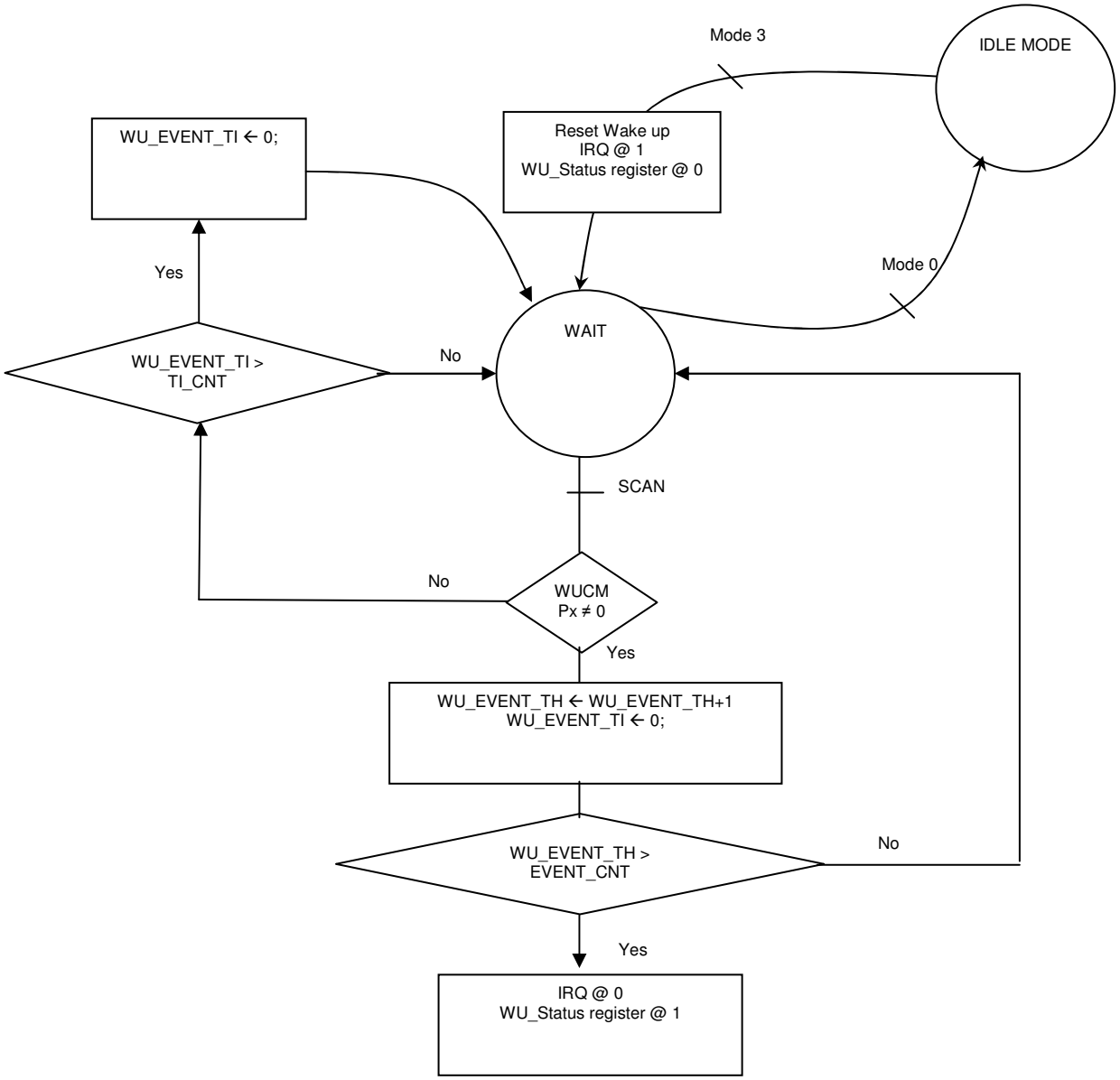
Wake Up (Refer to Wake up registers description)

The wake up mode is used to detect the first finger sweep on the sensor. The pixel array is switched off and only a specific pixel is used. The clock is supplied by an internal RC oscillator and dedicated to the very low consumption.
When a finger is detected, the FC108 generates an interruption on IRQ pin that can wakes up the host (or companion chip), the host will be able to immediately send a request to acquire a fingerprint, and so in the same sweep, the FC108 is able to wake up and send the corresponding fingerprint data on the MISO pin.

Functional Description
When the finger sweeps on the chip, ridge and valley series are detected. The signal is amplified and a state machine decides if the signal is compatible with a real fingerprint swipe. This method enables to automatically filter most unwanted possible wake up events such as unintentional touches, and saves power as the host will not be wake up on such events.



State Machine



Algorithm

- Event is WUCM High or Low detection.
- The first analyze start when the first event is detected.
- WU_EVENT_TH events need in WU_EVENT_TI time to declare a positive analyze.
- So a WAKE-UP is detected, IRQ is pushed to zero to activate an interruption. IRQ stays at 0 level as long as the FC108 is not in IDLE mode.

Acquisition and Navigation (Refer to Control register description)

These modes are activated by writing MODE bits into CTRL register (respectively MODE=0x1 or MODE=0x2).
For these 2 modes the mechanisms are the same. The only difference comes from the number of columns which are acquired:

- 192 columns are acquired in acquisition mode (the whole pixel plan)
- 128 columns (between columns 32 to 159) are acquired in navigation mode

After having activated one of these modes, the user has to acquire 5 dummy words (40 SCK pulses) before acquiring the first column (synchronization column):
In acquisition mode, a slice is acquired every 193x32 SCK clock pulses (192 columns + 1 dummy column).
In navigation mode, a slice is acquired every 129x32 SCK clock pulses (128 columns + 1 dummy column).

Warning: the user has to select idle mode before going from acquisition to navigation mode or before going from navigation to acquisition mode.

Navigation Mode

This mode allows user to extract navigation and click information from the 128*6 pixel matrix.
This extract is performed inside the host processor thanks to low level algorithm provided by Atmel.
The sensor itself does not embed any processing element for fingerprint reconstruction or click and navigation treatment. This is the role of the dedicated FingerChip Secure Processor or the associated companion chip. The sensor only sends the raw slices information to the companion chip.

Temperature management

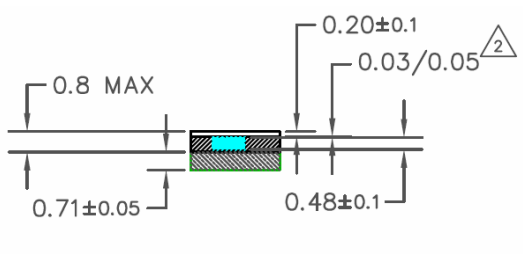
The sensor has an embedded temperature control unit. When the temperature difference between the sensor and the skin is increased, the images are more contrasted. This function is optional and its use depends on the quality of the image processing software. Therefore its management should be decided together with the image processing software.
In order to limit excessive current when a problem occurs, a watchdog implemented will stop the temperature management if not periodically (re)activated, after typically 4 seconds.
The temperature control function is a self regulated process that dissipates energy up to a selected level.
The heater can be switched:

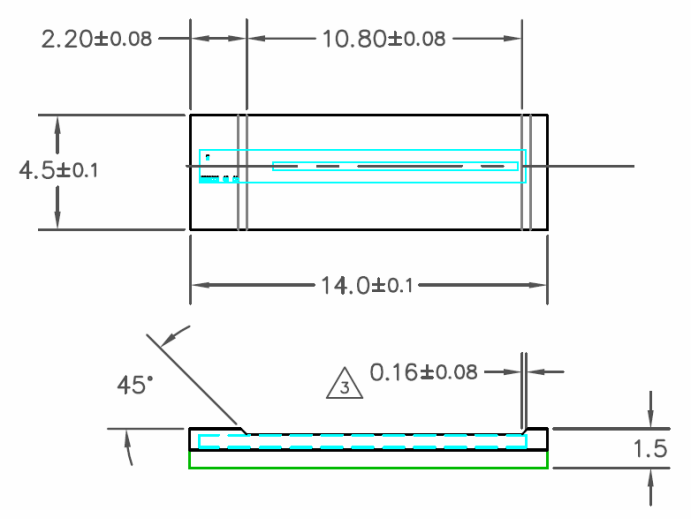
- OFF: No injected power
- ON: 60 mA regulated

Packaging Mechanical Data

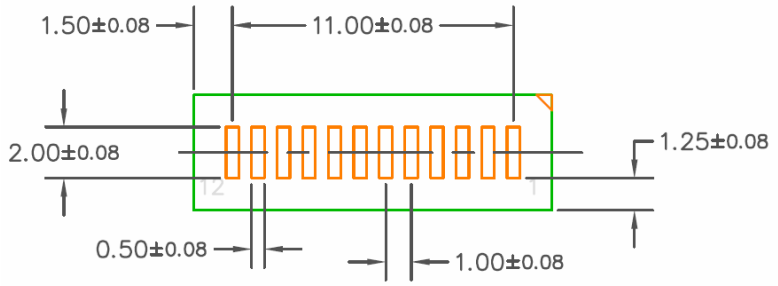
AT77C108A- XXXXI Package Information

AT77C108A- XXXXI Top View





AT77C108A- XXXXI Bottom View



TOLERANCES UNLESS NOTED	
DECIMAL	[mm]
.X ±.1	±0.1
.XX ±.01	±0.01
.XXX ±.005	±0.001
ANGLES ±1°	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS
2. DISTANCE FROM DIE SURFACE TO TOP OF MOLD COMPOUND
3. DISTANCE FROM END OF DIE TO BEGINNING OF MOLDED CHAMFER

Ordering Information

Package device